CLAIMS

1. A digital signal processor (1) comprising:
   an instruction memory (2), a central arithmetic unit 5, a register (4), a controller (3), and input/output devices;
   characterized in that
   - the instruction memory (2) is arranged to include time performance constraints and event;
   - the controller (3) is arranged to suspend further processing of time performance constraints after initiating operations in an event control unit (6);
   - the event control unit(6) is arranged to recognize an event and to control processing to be carried out as a consequence of the event while fulfilling the time performance constraints and
   - the controller (3) is arranged to resume processing when advised by the event control unit (6).

2. A digital signal processor (1) in accordance with claim 1, wherein the event is recognized in a detector and introduced as a level transition to the event control unit (6).

3. A digital signal processor (1) in accordance with claim 2, wherein the detector is arranged to detect input signals by determining the energy level in the signal.

4. A digital signal processor (1) in accordance with claim 2 or 3, wherein a further event is recognized as a completion of the processing carried out as a consequence of the previous event.

5. A digital signal processor (1) in accordance with claim 1, wherein the event is recognized as a completion of the processing carried out as a consequence of the previous event.

6. A digital signal processor (1) in accordance with claim 1, including a signal memory (7) arranged to store and extract data under control of the event control unit (6).

7. A digital signal processor (1) in accordance with claim 6, wherein the signal memory (7) is a vector memory with low granularity and where the granularity determines a split between a high-resolution part and a low-resolution part of the time performance constraints.

8. A digital signal processor (1) in accordance with claim 7, wherein the event control unit (6) is arranged to process the low-resolution part.

9. A digital signal processor (1) in accordance with claim 7, wherein the high-resolution part is processed during memory access to the signal memory (7) by delaying the access to the signal memory (7) a period of time corresponding to the high-resolution part..

10. A digital signal processor 1 in accordance with claim 1, including two or more event control units (6a, 6b) arranged to work independently from each other.